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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,693	BRITSON ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6 and 8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6.8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Response to the applicant's amendment dated 6/18 2007
- Claims 5 and 7 have been Cancelled
- Amended claims 1-4, 6 and 8-20 have been submitted for examination
- Amended claims 1-4, 6 and 8-20 have been rejected

Drawings Objections

1. In view of the applicant-amended drawings filed on 6/18/2007, all objections to the drawings are withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4, 6 and 8-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-4, 6, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watari US patent no. 4894708 (Hereinafter Watari) and in further view of Bunton et al. US patent no. 6961347 (Hereinafter Bunton).

4. In regard to claim 1, Watari teaches:

- (Currently Amended) A method for testing an integrated circuit (IC).comprising:

- employing one of a plurality of input lines to receive a test signal for a processor;

(Note: FIG. 2, reference characters (1), (1,1a), (8), (8a) and col. 3, lines (4-14) in Watari)

- employing one of a plurality of output lines to send a test result from the processor; and

(Note: FIG. 2, reference characters (1), (1,1a), (8), (8a) and col. 3, lines (4-14) in Watari)

- if the test result is unsuccessful, performing at least one of:

(Note: col. 3, lines (23-26) in Watari)

However, Watari does not teach:

- selecting and automatically switching to a remaining one of the plurality of input lines to receive the test signal for the processor using a first selection signal; and

- selecting and automatically switching to a remaining one of the plurality of output lines to send the test result from the processor using a second selection signal.

Bunton in an analogous art that teaches high-speed interconnection link having automated lane reordering teaches:

- selecting and automatically switching to a remaining one of the plurality of input lines to receive the test signal for the processor using a first selection signal; and

(Note: FIG. 9 and col. 10, lines (28-58) in Bunton)

- selecting and automatically switching to a remaining one of the plurality of output lines to send the test result from the processor using a second selection signal.

(Note: FIG. 9 and col. 10, lines (28-58) in Bunton)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Bunton that comprise automatic switching of input/output lines (pins) with the teaching of Watari.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need for automatically correcting backplanes and input/output IC pins.

5. In regard to claim 2, Watari teaches:

- applying the test signal to each of the plurality of input lines;

(Note: FIG. 2, any of reference characters ((1), (1 ,la), (8), (8a) in Watari)

- selecting one of the plurality of input lines; and (Note: FIG. 2, reference character (8a) in Watari)

receiving the test signal for the processor from the selected input line. (Note: FIG. 2, reference character (8a) in Watari)

6. In regard to claim 3, Watari teaches:

- applying the test result to each of the plurality of output lines;

(Note: FIG. 2, any of reference characters ((1), (1,1a), (8), (8a) in Watari) - selecting one of the plurality of output lines; and (Note: FIG. 2, reference character (8a) in Watari)

- sending the test result from the processor using the selected output line.

(Note: FIG. 2, reference character (8a) in Watari)

7. In regard to claim 4, Watari teaches:

- selecting a remaining one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of input lines to receive the test signal.

(Note: FIG. 2, reference character (8a) in Watari)

8. In regard to claim 6, Watari teaches:

- selecting a remaining one of the plurality of output lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: FIG. 2, reference character (8a) in Watari)

9. In regard to claim 8, Watari teaches:

- employing a remaining one of the plurality of input lines to receive the test signal for the processor includes:

- selecting a remaining one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of input lines to receive the test signal; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing a remaining one of the plurality of output lines to send the test result from the processor includes:

selecting a remaining one of the plurality of output lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employing the selected remaining one of the plurality of output lines to send the test result from the processor.

(Note: FIG. 2, reference character (8a) in Watari)

10. In regard to claim 10, Bunton teaches:

- (Currently Amended) An apparatus for testing an IC comprising:

  a processor within the IC;

- a plurality of input lines coupled to the processor positioned internally within the IC;

(Note: Any of FIG. 10 or FIG. 11, The input/output lines are within the IC on the 4 LANE TRANSMITTER/RECEIVER in reference characters (1000) and (1010) in Bunton)

- a plurality of output lines coupled to the processor positioned internal within the IC; and

(Note: Any of FIG. 10 or FIG. 11, The input/output lines are within the IC on the 4 LANE TRANSMITTER/RECEIVER in reference characters (1000) and (1010) in Bunton)

- a connector interface coupled to the plurality of input lines and the plurality of output lines;

- wherein the apparatus is adapted to:

- employ one of the plurality of input lines to receive a test signal for the processor;

(Note: FIG. 2, reference characters (1), (1,1a), (8), (8a) and col. 3, lines (4-14) in Watari)

- employ one of the plurality of output lines to send a test result from the processor; and

(Note: FIG. 2, reference characters (1), (1,1a), (8), (8a) and col. 3, lines (4-14) in Watari)

- if the test result is unsuccessful, perform at least one of:

- selecting and automatically switching to a remaining one of the plurality of input lines to receive the test signal for the processor using a first selection signal; and

(Note: FIG. 9 and col. 10, lines (28-58) in Bunton)

- selecting and automatically switching to a remaining one of the plurality of output lines to send the test result from the processor using a second selection signal.

(Note: FIG. 9 and col. 10, lines (28-58) in Bunton)

11. Claims 9 an 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watari/Bunton as applied to claim 8 above, and further in view of Bombai et al. US patent no. 6141782 (Hereinafter Bombai).

12. In regard to claim 9, Watari/Bunton teaches substantially all the limitations in claim 8.

However, Watari/Bunton do not teach

- selecting a remaining one of the plurality of input lines includes: modifying a first select signal; and
- selecting a remaining one of the plurality of input lines based on the modified first select signal; and
- modifying a second select signal; and
- selecting a remaining one of the plurality of output lines based on the modified second select signal.

Bombai in an analogous art that teaches pseudo-scan using hardware accessible IC structures teaches:

- selecting a remaining one of the plurality of input lines includes: modifying a first select signal; and

(Note: FIG. 8, third block in Bombai) and

- selecting a remaining one of the plurality of input lines based on the modified first select signal; and

(Note: FIG. 2, reference character (8a) in Watari)

- modifying a second select signal; and

(Note: FIG. 8, third block in Bombai) and

- selecting a remaining one of the plurality of output lines based on the modified second select signal.

(Note: FIG. 2, reference character (7a) in Watari)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Watari that teaches parallel I/0 testing of an IC with the teaching of Bombai.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need for an efficient IC fault coverage.

13. Claim 19 is rejected for the same reasons as per claim 9.

14. Claims 11-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watari/Bunton as applied to claim 10 above, and further in view of Evans US publication no. 2003/0208713 (Hereinafter Evans).

15. In regard to claim 11, Watari substantially teaches all the limitations in claim 10. However, Watari/Bunton do not teaches:

- The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and
- further comprising a first multiplexer coupled to the plurality of input lines and the processor, and adapted to:

- select one of the plurality of input lines; and

- receive the test signal for the processor on the selected input line.

Evans in an analogous art that teaches a test head performs at-speed testing of high serial pin count devices teaches:

- The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and further comprising a first multiplexer coupled to the plurality of input lines and the processor, and adapted to:

(Note: FIG. 10, reference character (312A)in Evans)

- select one of the plurality of input lines; and

(Note: FIG. 10, reference character (114C) in Evans)

- receive the test signal for the processor on the selected input line. (Note: FIG. 10, reference character (810) in Evans)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Watari/Bunton that teaches parallel I/O testing of an IC with the teaching of Evans.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to minimize IC line failures.

16. In regard to claim 12, Watari teaches:

- select a remaining one of the plurality of input lines; and

(Note: FIG. 2, reference character (8a) in Watari)

- employ the selected remaining one of the plurality of input lines to receive the test signal.

(Note: FIG. 2, reference character (8a) in Watari)

17. In regard to claim 13, Evans teaches:

- The apparatus of claim 11 further comprising a third multiplexer coupled to the connector interface and first multiplexer, and adapted to modify a first select signal, the first select signal corresponding to the first multiplexer; and

(Note: FIG. 8, third block in Bombai) and FIG. 10, reference character (308) in Evans)

- wherein the first multiplexer is further adapted to select a remaining one of the plurality of input lines based on the modified first select signal.

(Note: FIG. 10, reference character (312A) in Evans)

In regard to claim 14, Evans teaches:

- The apparatus of claim 10 wherein the processor is adapted to apply the test result to each of the plurality of output lines; and

- further comprising a second multiplexer coupled to the plurality of output lines and the connector interface, and adapted to:

(Note: FIG. 10, reference character (308) in Evans)

- select one of the plurality of output lines; and

- send the test result from the processor using the selected output line.

(Note: FIG. 10, reference character (114C)in Evans)

18. Claim 15 is rejected for the same reasons as per claim 12.

19. Claim 16 is rejected for the same reasons as per claim 13.

20. In regard to claim 17, Evans teaches:

- The apparatus of claim 10 wherein the connector interface is adapted to apply the test signal to each of the plurality of input lines; and further comprising a first multiplexer coupled to the plurality of input lines and the processor, the first multiplexer adapted to:

(Note: FIG. 10, reference character (312A) in Evans)
select one of the plurality of input lines; and

receive the test signal for the processor from the selected input line;
(Note: FIG. 10, reference character (810) in Evans)

- wherein the processor is further adapted to apply the test result to each of the plurality of output lines; and
- further comprising a second multiplexer coupled to the plurality of output lines and the connector interface, the second multiplexer adapted to:

(Note: FIG. 10, reference character (308) in Evans)
- select one of the plurality of output lines; and

- send the test result from the processor using the selected output line.

(Note: FIG. 10, reference character (308) in Evans)

21. Claim 18 is rejected for the same reasons as per claim 15

22. In regard to claim 20, Evans teaches:

- The apparatus of claim i0 wherein the connector interface is adapted to couple to a service processor.

(Note: FIG. 1A, reference character (102) in Evans)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk,

Examiner

ART UNIT 2112

8/1/07

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